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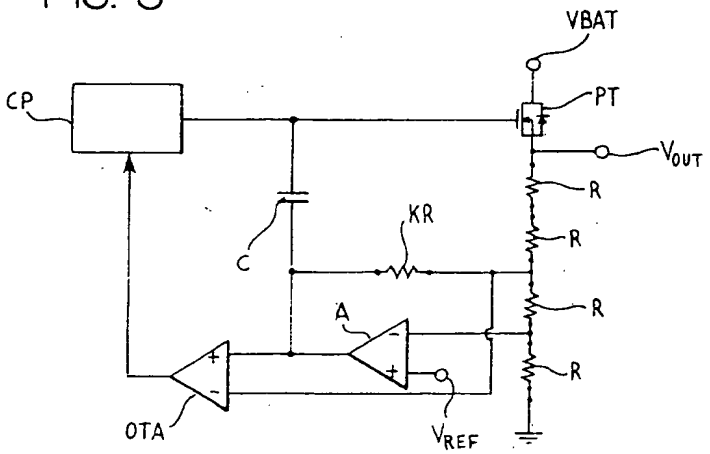
(54) Power transistor control circuit for a voltage regulator

(57) A voltage-regulator circuit with a low voltage drop using a DMOS power transistor (PT) driven by a charge pump (CP) comprises two feedback loops: a first feedback loop having high gain and accuracy but low response speed, and a second feedback loop having a wide passband and fast response speed but low gain.

FIG. 3



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Description

The present invention relates, in general, to circuits for controlling power transistors in a voltage regulator. More specifically, this invention relates to a circuit for controlling power transistors in a linear voltage regulator with a low voltage drop.

Currently, there is an ever greater requirement by the market for voltage regulators with low voltage drop, that is, regulators which can operate correctly even if the voltage drop between the supply voltage and the regulated output voltage is a fraction of a volt. These linear voltage regulators with low voltage drop are required for various reasons.

They improve efficiency in both battery-operated electronic systems and those operating with a mains supply. A regulator which supplies an output voltage of 5V and needs a voltage drop of 5V has an efficiency of 50% whereas, if it requires a voltage drop of only 0.5V between the input and the output, its efficiency is more than 90%.

A reduction in the power dissipated by the regulator avoids the use of large dissipators and enables less expensive housings to be used. A regulator which requires a voltage drop of 5V when it is supplying a current of 1A to the load has to dissipate a power of 5W; with a voltage drop of 0.5V, it has to dissipate only 0.5W. The reduction in the dimensions of the dissipator, or its elimination, and the reduction in the dimensions of the transformer (in mains applications) also permits a considerable saving of space.

The continual reduction of the supply voltages of electronic devices with the consequent spread of systems with a mixed 5V and 3.3V supply (the latter can be produced from the former simply by a regulator with a low voltage drop) necessitates the use of regulators of this type.

Moreover, these regulators supply a constant voltage to the load even in motor-vehicle applications in which the voltage supplied by the battery may fluctuate considerably because of changes in temperature or in the load currents. An example is the starting of the motor-vehicle at low temperature, in which situation the battery voltage may fall to values little greater than 5V.

The element around which a voltage regulator is constructed may be a bipolar transistor or a MOS power transistor. In the first case, the minimum voltage drop is given by the saturation voltage V_{sat} of the transistor. In the second case, the minimum voltage drop between input and output is related to the voltage Vgs supplied between the gate and source terminals and to the physical size of the transistor, and the voltage drop could thus be reduced even to a few tens of millivolts. Another advantage of MOS transistors, for example, those of the DMOS type, is the smaller area of silicon occupied.

However, problems arise if it is attempted to produce a wholly integrated regulator which minimises, or reduces to zero, the number of external components necessary for the regulator to be functional and stable and to have a rapid response to changes in the voltage regulated, with performance comparable to or better than normal regulators without a low drop. One of the main problems is that the gate voltage of the MOS transistor has to be brought to high values, usually to a voltage greater than the supply voltage.

Solutions according to the prior art use a charge pump to generate a voltage high enough to be able to drive the MOS power transistor. A solution of this type is shown in Figure 1.

The voltage-regulator circuit shown uses a charge pump CP which supplies a voltage greater than that provided at an input IN of the voltage regulator. This voltage supplied by the charge pump CP supplies an output stage BUF of an error amplifier ERA which in turn controls a gate terminal of a power transistor PT.

The other main terminals of the voltage regulator are also indicated in Figure 1. Thus, the output terminal OUT, the earth terminal GND and the adjustment terminal ADJ can be seen. As can be noted, the control loop of the voltage regulator is conventional, the non-inverting and inverting inputs of the error amplifier ERA being connected to a band-gap voltage reference BG and to the adjustment terminal ADJ, respectively. The drawing also shows a fold-back protection circuit FB. The other parts of the circuit of Figure 1 are not described since they are not relevant for the purposes of the present invention.

The object of the present invention is to provide a linear voltage-regulator circuit with a low drop which solves all of the problems indicated above in a satisfactory manner.

According to the present invention, this object is achieved by means of a linear voltage-regulator circuit with a low drop having the characteristics indicated in the claims following the present description.

Further advantages and characteristics of the present invention will become clear from the following detailed description, given with the aid of the appended drawings, provided by way of non-limiting example, in which:

Figure 1 is a diagram of a circuit according to the prior art and has already been described,

Figures 2 to 4 are diagrams of three alternative embodiments of the circuit according to the invention,

Figure 5 is a cartesian graph showing the operation of the circuits shown in Figures 2 to 4,

Figure 6 is a diagram of a further alternative embodiment of the circuit according to the invention,

Figure 7 is a cartesian graph showing the operation of the circuit shown in Figure 6,

Figure 8 is a diagram of a further alternative embodiment of the circuit according to the invention.

A simplified diagram of the voltage regulator according to the invention is shown in Figure 2. As can be seen, the circuit shown in Figure 2 comprises a power transistor PT, for example, a DMOS transistor, supplied by an input voltage VBAT and having the function of regulating an output voltage Vout in a manner such that it adopts a predetermined value. As in the prior art, the gate terminal of the power transistor PT is driven directly by a charge pump CP.

Naturally, the circuit operates with a closed loop using, as the feedback signal, a signal indicative of the output voltage Vout obtained by means of a resistive divider constituted by four resistors R interposed between the output and the earth of the circuit. This signal, which is indicative of the output voltage Vout, is compared with a predetermined reference voltage Vref in order to generate a control signal for the gate terminal of the power transistor PT according to a conventional layout for closed-loop regulation systems.

The other elements which make up the feedback loop are two amplifiers OTA and G and a capacitor C. The operation of this feedback loop, which differs from the circuits of the prior art, will now be described.

To obtain the output voltage which, in the specific case, is 5V, the reference voltage Vref which, in the specific case, is 1.25 V and is produced, for example, by means of a band-gap circuit, is multiplied by four with the use of the resistive divider constituted by the four resistors R. The current of the MOS power transistor PT is controlled by means of a double feedback: a first, direct-current feedback by means of the two amplifiers G, OTA in cascade and the charge pump CP and a second, frequency feedback with the use of the first amplifier G and the capacitor C.

The voltage-regulator circuit according to the invention thus actually comprises two feedback loops. The first feedback loop comprises the power transistor PT, the resistive divider R, the first amplifier G, the second amplifier OTA, and the charge pump CP. The second feedback loop, on the other hand, comprises the power transistor PT, the resistive divider R, the first amplifier G, and the capacitor C.

The charge pump CP which may, for example, be a voltage tripler, is used to bring the gate terminal of the power transistor PT to voltages greater than the supply voltage VBAT.

The current in the charge pump CP is controlled by the first feedback loop, that is, by means of the first amplifier G, followed by the second amplifier OTA. This amplifier OTA, is, for example, a transconductance operational amplifier. When the output voltage Vout is in the steady state, the second amplifier OTA no longer supplies current to the charge pump CP, which is turned off.

The high loop gain of the first feedback loop leads to great precision in the regulation of the output voltage Vout.

In order to save silicon area, small capacitors may be used in the charge pump CP; in a circuit produced by the Applicant, for example, they are of one order of magnitude lower than the parasitic capacitances of the DMOS transistor PT. The small current injected into the gate terminal by the charge pump CP, added to the high parasitic capacitances at the gate terminal of the DMOS transistor PT, creates a pole at a low frequency which renders the first feedback loop quite slow. This problem is solved by the second feedback loop.

The second feedback loop is constituted by the first amplifier G which has a low gain and a wide band, and by the capacitor C. In this case, the loop gain is lower but the wide band enables the amplifier G to react quickly to any variations of the output voltage Vout, injecting charge into the gate terminal, or absorbing it by means of the capacitor C. For the circuit to operate well, this capacitor C must be of a size such as to be of the same order of magnitude as the parasitic capacitances present at the gate terminal of the DMOS transistor PT. The gate voltage is thus quickly brought close to the correct value which it can then reach precisely by virtue of the slower contribution of the first feedback loop.

Figure 3 shows an embodiment of the voltage-regulator circuit according to the invention in which a possible embodiment of the low-gain, wide passband amplifier is shown. The operational amplifier A used has a feedback network constituted by two resistances of the output divider and by a resistor of value KR, where K is a constant.

In this configuration, the intermediate node of the divider behaves as a virtual earth at a voltage equal to 2 V_{REF}.

Any departure of the output from its nominal value is amplified by a factor

$$\frac{K}{2} = \frac{KR}{2R}$$

The relationship between this factor and the gain G of Figure 2 is as follows:

$$\frac{K}{2} = \frac{G}{4} \text{ or } K = \frac{G}{2}$$

As can be seen, the inverting input of the second amplifier OTA is connected to a reference voltage such as to polarize the output of the amplifier A to a voltage $2V_{REF}$.

In the steady state, the current passing through the resistor KR is thus zero and, in the specific embodiment, the output range of the amplifier A is maximized.

Figure 4 is a detailed diagram of the current-control of the charge pump. The second amplifier OTA operates as a switch and two transistors B1 and B2 operate as current buffers. It should be noted that the latter are polarized in a manner such that, when the output volt-

age Vout is in the steady state they are both switched off and the current supplied to the charge pump CP or absorbed by the gate terminal of the DMOS transistor PT is zero.

The two feedback loops also ensure the stability of the circuit. The Bode diagram of the loop gain resulting from the combination of the two loops is given in Figure 5. This diagram shows the loop gain 'Av' of the circuit, expressed in dB, as a function of the frequency f, expressed in Hz.

The dominant pole P_1 is produced with the use of the parasitic capacitances of the DMOS power transistor PT. A second pole P_2 is given by the operational amplifier G. The circuit also has a zero z_1, which is important for compensating for a pole P_{OUT} which is introduced by the load capacitance at the output and the frequency of which is shifted with variations of the current supplied by the regulator. In fact, the pole P_{OUT} can be expressed as:

$$P_{out} = \frac{gm_{DMOS} + \frac{1}{R_{LOAD}}}{C_{LOAD}}$$

Where C_{LOAD} and R_{LOAD} are the load capacitance and resistance, respectively. Owing to the large dimensions of the DMOS transistor PT, $gm_{DMOS} >> 1/R_{LOAD}$ and, as a first approximation, the pole P_{out} can thus be expressed as:

$$P_{out} \cong \frac{gm_{DMOS}}{C_{LOAD}}$$

When the pole P_{out} varies, the loop gain is modified as indicated by the broken line in Figure 5. If the pole P_{out} coincides with one of the singularities z_1 or p_2 it is necessary to ensure a phase margin which is adequate for the stability of the circuit by accurate dimensioning of the feedback resistor KR. In doing this, it is necessary also to bear in mind the capacitive divider constituted by the capacitor C and by the parasitic capacitances of the DMOS power transistor PT which lead to an attenuation of the loop gain, possibly of more than 10dB.

Figure 6 is a simplified diagram of an alternative embodiment of the circuit. The charge pump CP and the capacitor C are used in a similar manner. The differences lie in the feedback loop which is formed by a single operational amplifier A which controls both the feedback capacitor C and the current supplied by the charge pump CP. In this embodiment, the same operational amplifier A provides both the high, direct-current gain and the low gain and wide passband at high frequency. In order to polarize the output of the operational amplifier A to a voltage of Vref/2 and to introduce the frequency zero z_1 it was necessary to add a further capacitor C_R.

In this embodiment, the two feedback loops also ensure stability of the circuit, the Bode diagram of the loop gain resulting from the combination of the two loops is given in Figure 7. In this case, the zero z_1 is introduced by the feedback network of the operational amplifier A. For the rest of the circuit, comments similar to those made above may be made.

Figure 8 shows in detail the current switch controlled by the operational amplifier A. The transistors B1 and B2 are polarized in a manner such that the output of the operational amplifier A is at a voltage of about Vref/2 to maximise the range. A resistor R1 is required to limit the current supplied to the charge pump CP by the output stage of the operational amplifier A.

A characteristic of MOS transistors is that they have a high parasitic capacitance between the gate terminal and the source terminal. The charge pump CP sends charge to the gate terminal in a pulsed manner which leads to interference which appears at the source terminal in the form of a voltage wave. The use of small capacitances and the switching-off of the charge pump CP in the steady state prevent this problem whilst the wide-band feedback loop at the same time ensures a quick response of the regulator circuit to external stresses.

As can therefore be seen, the voltage-regulator circuit according to the present invention has various important advantages which will be summarised below.

No storage capacitor is necessary in the charge pump CP, with a consequent saving of area.

The regulator does not require a compensation capacitor. The dominant pole is created by utilization of the parasitic capacitances of the MOS power transistor PT.

Independence from the pole introduced by the load is achieved without the need to limit the response speed of the regulator by over-compensation.

Naturally, the principle of the invention remaining the same, the details of construction and forms of embodiment may be varied widely with respect to those described and illustrated, without thereby departing from the scope of the present invention as defined in the annexed claims.

Claims

1. A voltage-regulator circuit comprising a power transistor (PT) which is supplied with an input voltage (VBAT) and can regulate an output voltage (Vout) of the regulator circuit, and a voltage-raising circuit (CP), which is supplied with the input voltage (VBAT) and can drive a control terminal of the transistor (PT), the voltage-raising circuit (CP) operating in dependence on a difference between a signal indicative of the output voltage (Vout) and a predetermined reference voltage (Vref),
characterized in that the regulator circuit operates in a closed loop with two feedback loops, a first

feedback loop having high gain and low response speed, and a second feedback loop having low gain, wide passband, and quick response.

2. A circuit according to Claim 1, characterized in that the first feedback loop comprises:

   - said power transistor (PT),
   - a resistive divider (R) for detecting the signal indicative of the output voltage (Vout),
   - a first amplifier (G),
   - a second amplifier (OTA), and
   - said voltage-raising circuit (CP).

3. A circuit according to Claim 1 or Claim 2, characterized in that the second feedback loop comprises:

   - said power transistor (PT),
   - said resistive divider (R) for detecting the signal indicative of the output voltage (Vout),
   - said first amplifier (G), and
   - a capacitor (C) connected between the output of the first amplifier (G) and a control terminal of the power transistor (PT).

4. A circuit according to Claim 2 or Claim 3, characterized in that the second amplifier (OTA) is a transconductance operational amplifier.

5. A circuit according to Claim 1, characterized in that the first feedback loop comprises:

   - said power transistor (PT),
   - a resistive divider (R) for detecting the signal indicative of the output voltage (Vout),
   - an operational amplifier (A), and
   - said voltage-raising circuit (CP).

6. A circuit according to Claim 1 or Claim 5, characterized in that the second feedback loop comprises:

   - said power transistor (PT),
   - said resistive divider (R) for detecting the signal indicative of the output voltage (Vout),
   - a capacitor (C) connected between the output of the operational amplifier (A) and a control terminal of the power transistor (PT), and
   - a further capacitor (C_R) connected between the resistive divider (R) and the output of the operational amplifier (A).

7. A circuit according to Claim 6, characterized in that the second feedback loop also comprises a further resistor (KR) connected in series with the further capacitor (C_R).

8. A circuit according to any one of Claims 1 to 7, characterized in that it comprises a circuit (B1, B2) which drives the voltage-raising circuit (CP) and which can switch off the voltage-raising circuit (CP) when the output voltage (Vout) is in the steady state.

9. A circuit according to any one of Claims 1 to 8, characterized in that the voltage-raising circuit (CP) is a voltage tripler circuit.

10. A circuit according to any one of Claims 1 to 9, characterized in that the capacitor (C) has a capacitance of the same order of magnitude as the parasitic capacitance of the power transistor (PT).

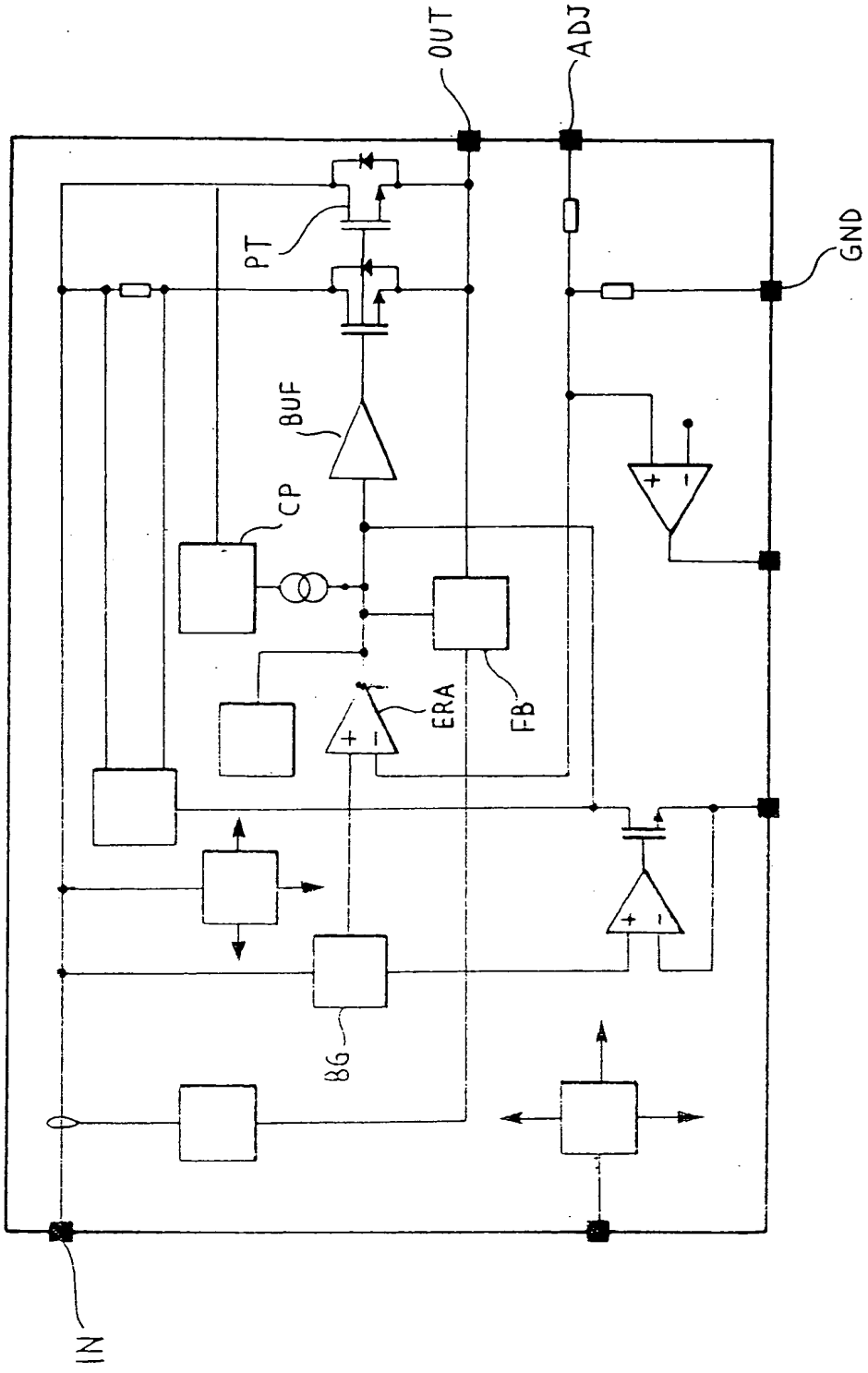


FIG. 1

FIG. 2

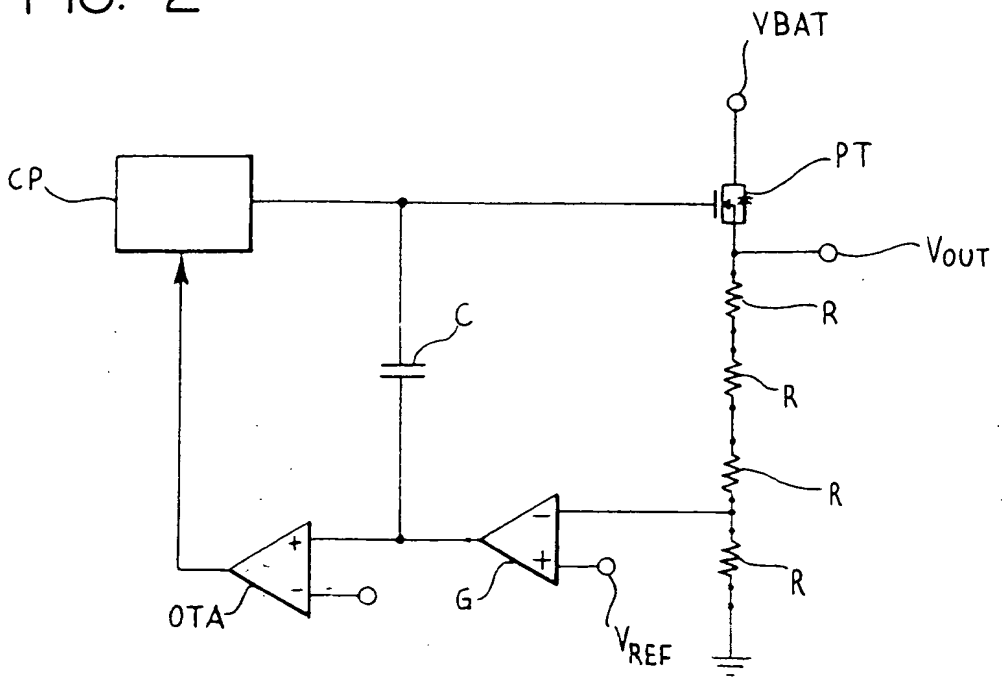
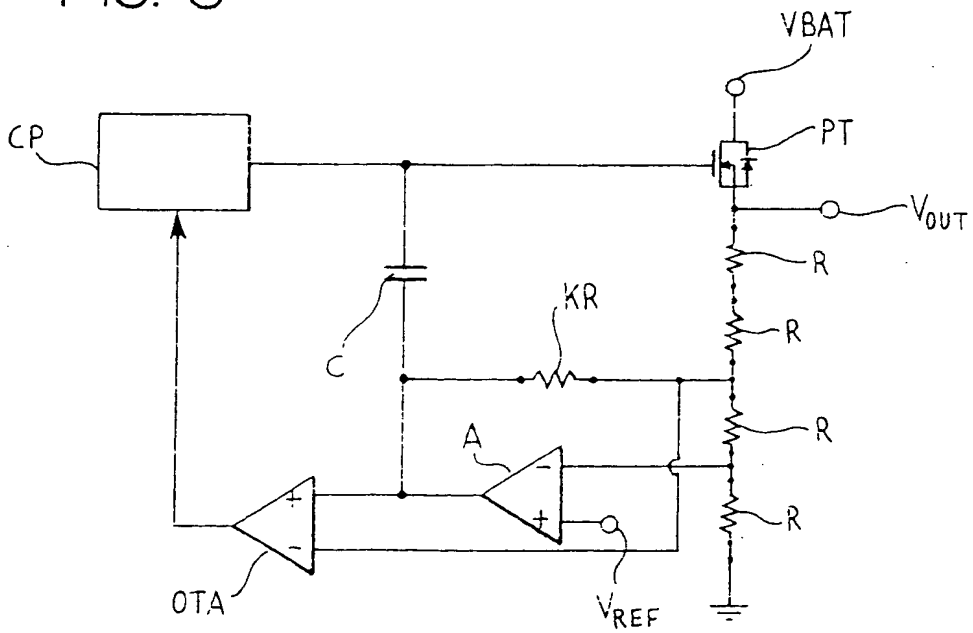

VBAT
PT
CP
VOUT
C
R
R
R
R
OTA
G
VREF

FIG. 3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PT
CP
VOUT
R
KR
R
C
A
R
R
OTA
VREF

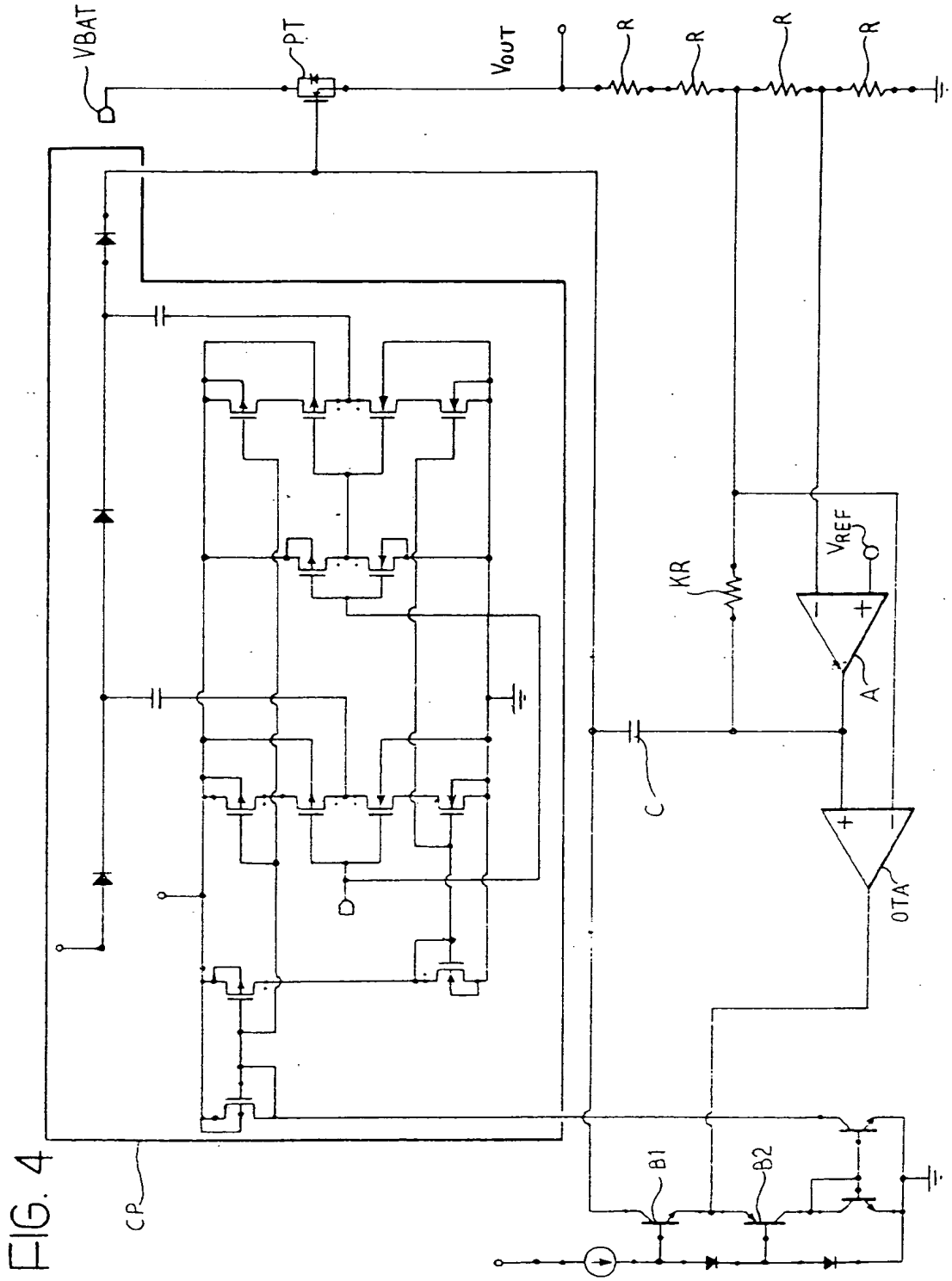


FIG. 4

FIG. 5

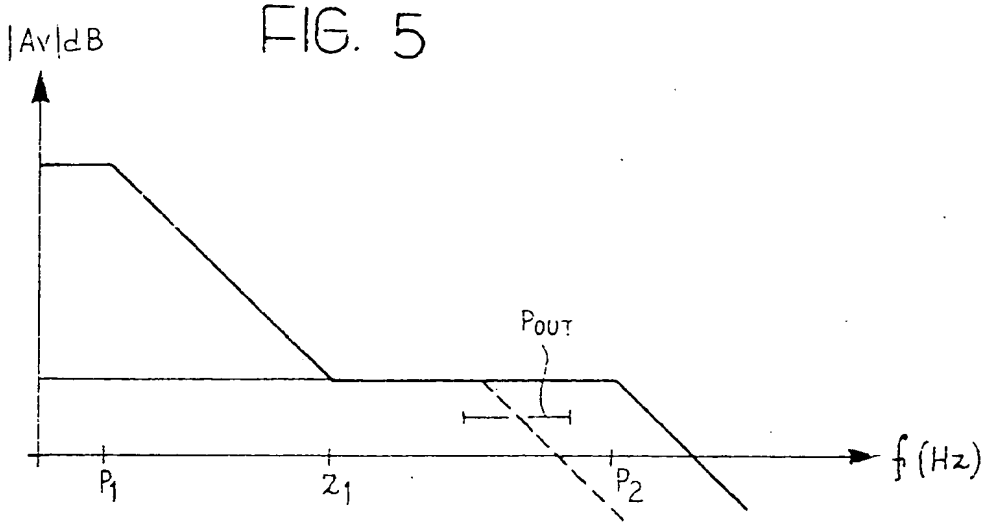


FIG. 6

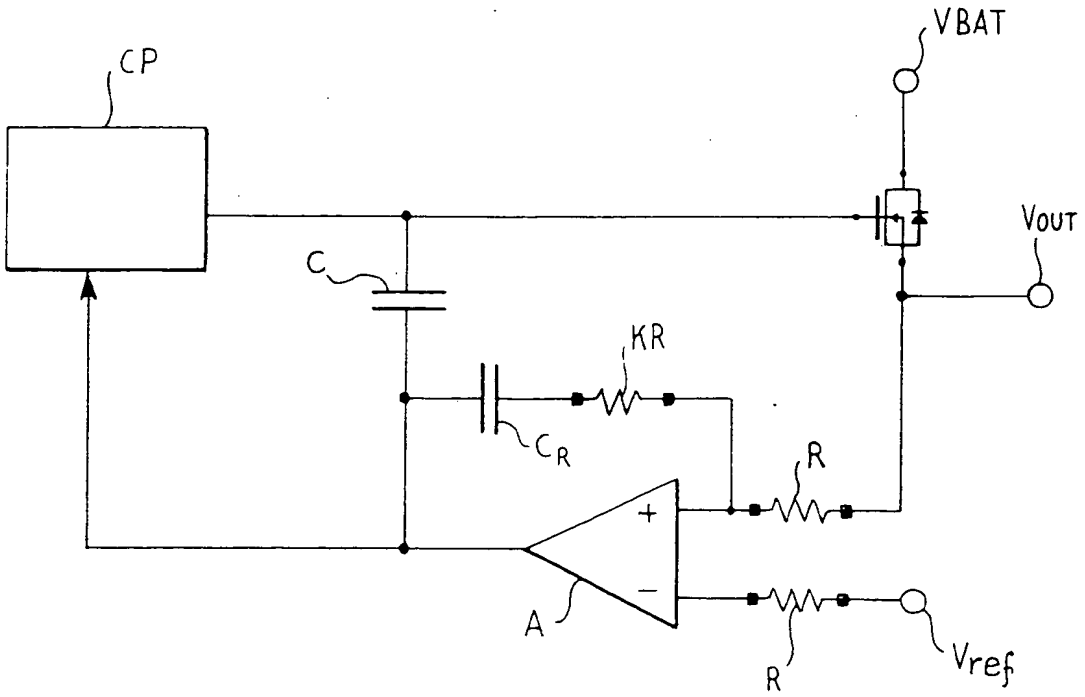


FIG. 7

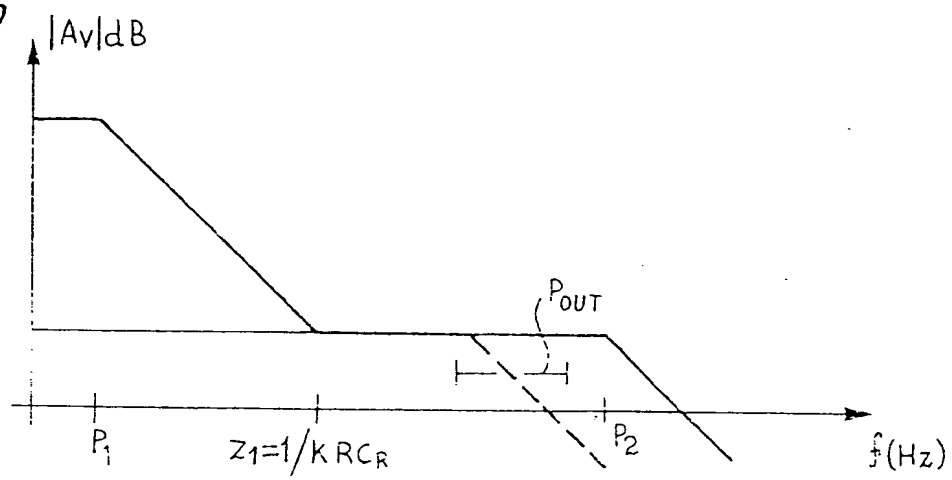
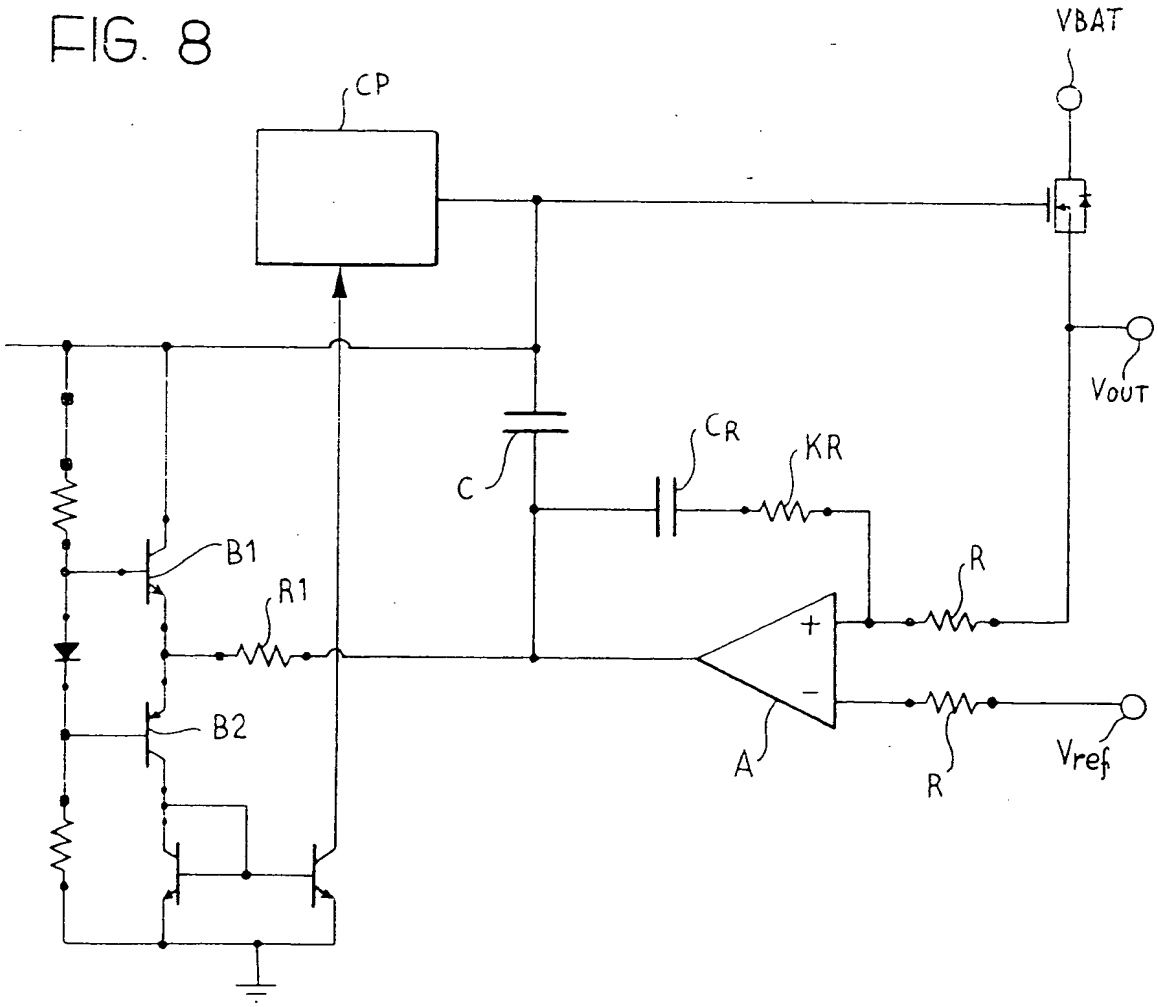

|Av|dB
POUT
P1
Z1=1/KRCR
P2
f(Hz)

FIG. 8


VBAT
CP
VOUT
C
CR
KR
B1
R1
R
B2
A
R
Vref

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 83 0610

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US 5 552 697 A (CHAN SHUFAN) 3 September 1996 * the whole document *	1-10	G05F1/575
Y	EP 0 499 921 A (SGS THOMSON MICROELECTRONICS) 26 August 1992 * the whole document *	1-10	
Y	WO 95 27239 A (NORTHERN TELECOM LTD) 12 October 1995 * abstract; figure 3 *	4	
A	EP 0 379 454 A (SGS THOMSON MICROELECTRONICS) 25 July 1990 * the whole document *	1-10	
A	EP 0 476 365 A (MOTOROLA JAPAN) 25 March 1992 * column 1, line 12 - column 2, line 44 *	1	
A	US 5 191 278 A (CARPENTER BRIAN A) 2 March 1993 * the whole document *	1-10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G05F
A	US 4 803 612 A (SKOVMAND TIMOTHY J) 7 February 1989 * abstract *	1	
A	EDN ELECTRICAL DESIGN NEWS, vol. 38, no. 12, 10 June 1993, pages 137-142, 144, 146, 148, XP000382987 JUNG W ET AL: "ANALOG CIRCUITS BYPASS SINGLE-SUPPLY DESIGN CONSTRAINTS" * the whole document *	1-10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 May 1997	Schobert, D

CATEGORY OF CITED DOCUMENTS

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